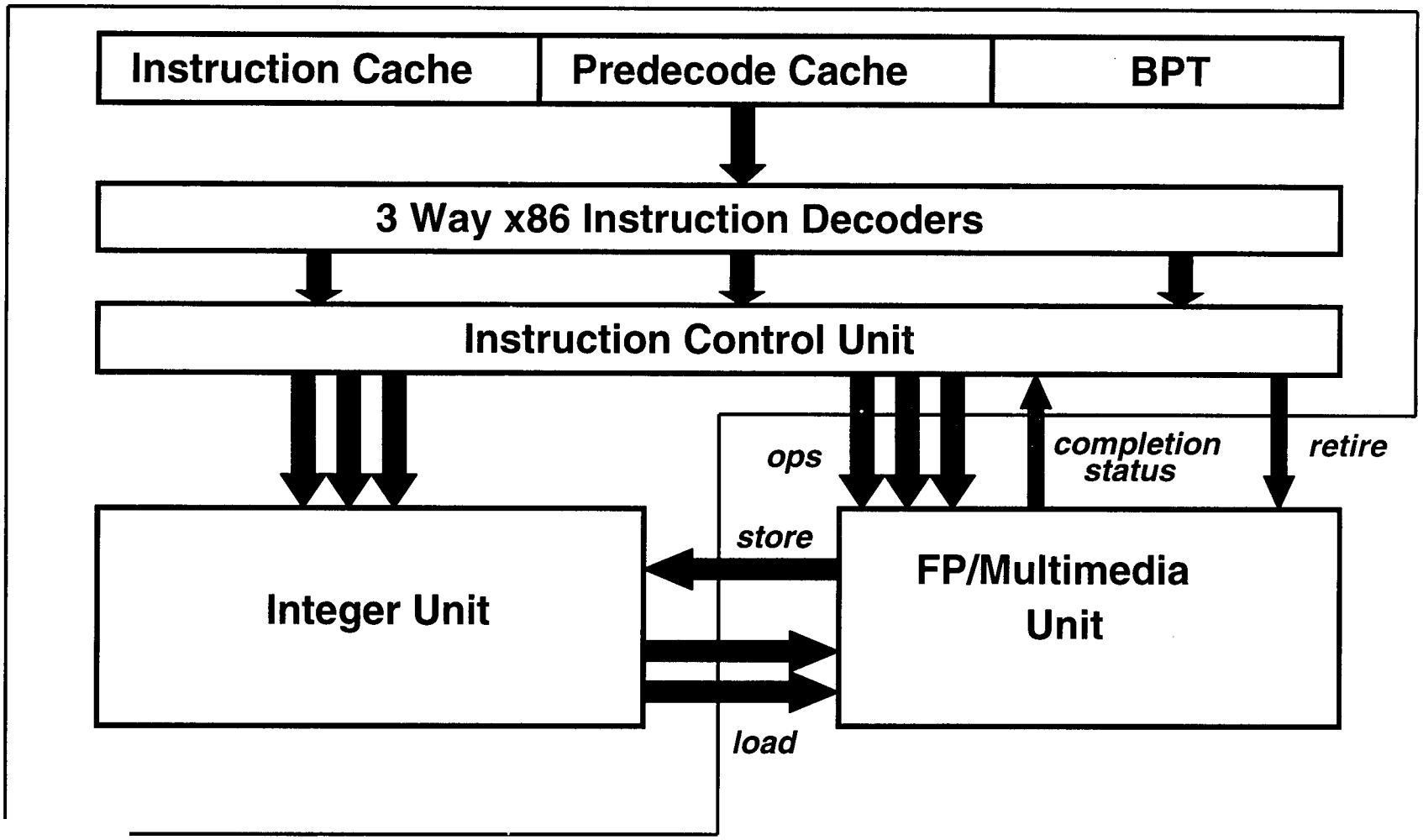
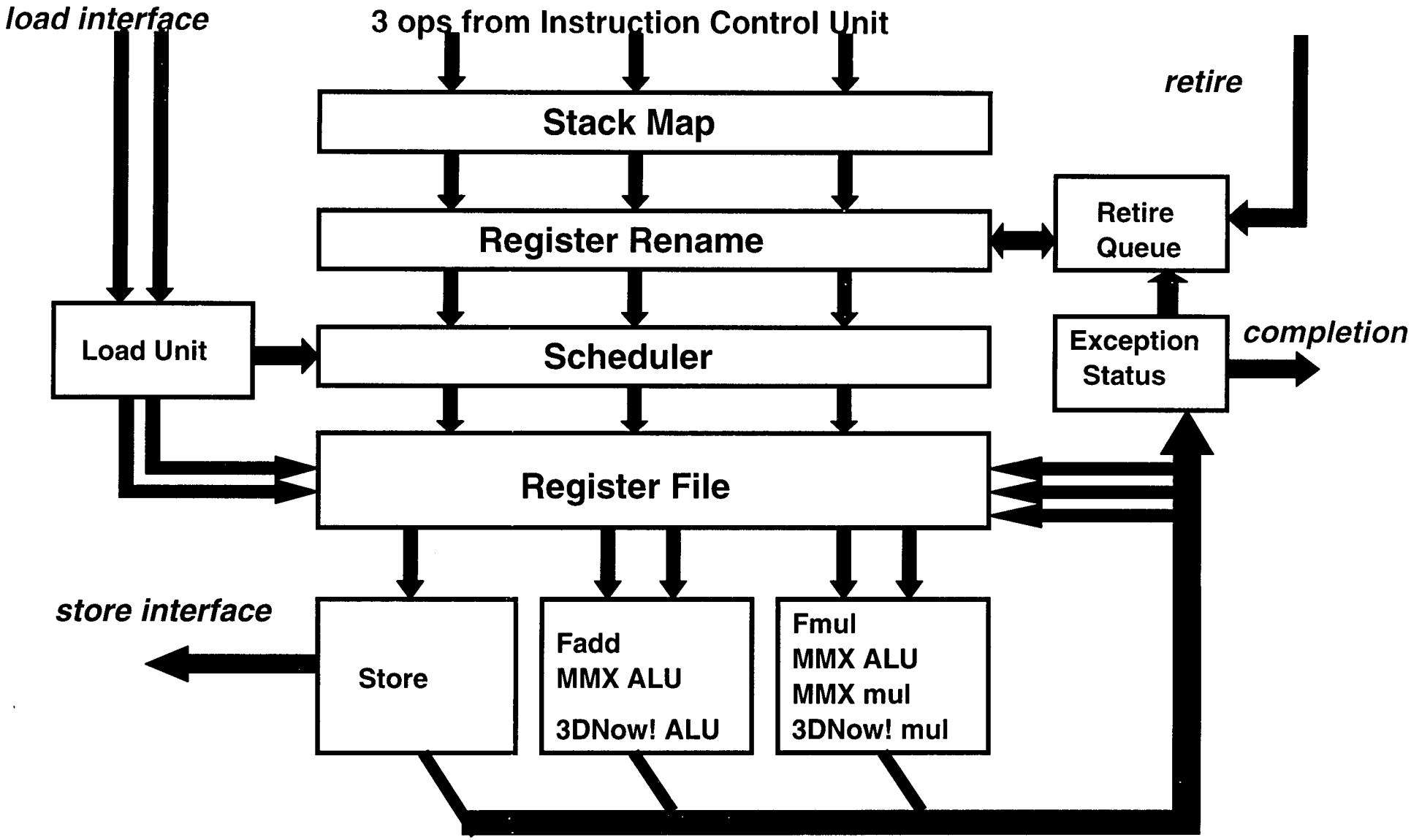
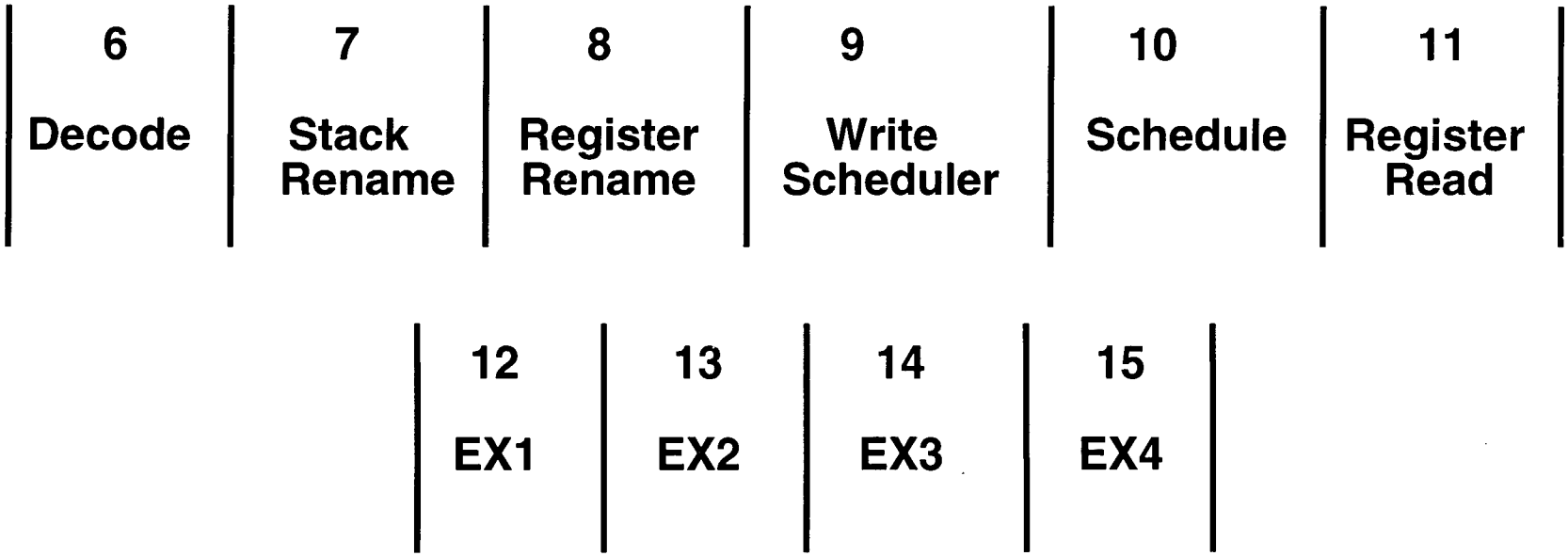
Coprocessor Model



Floating-Point Multimedia Block Diagram



Floating-Point Pipeline

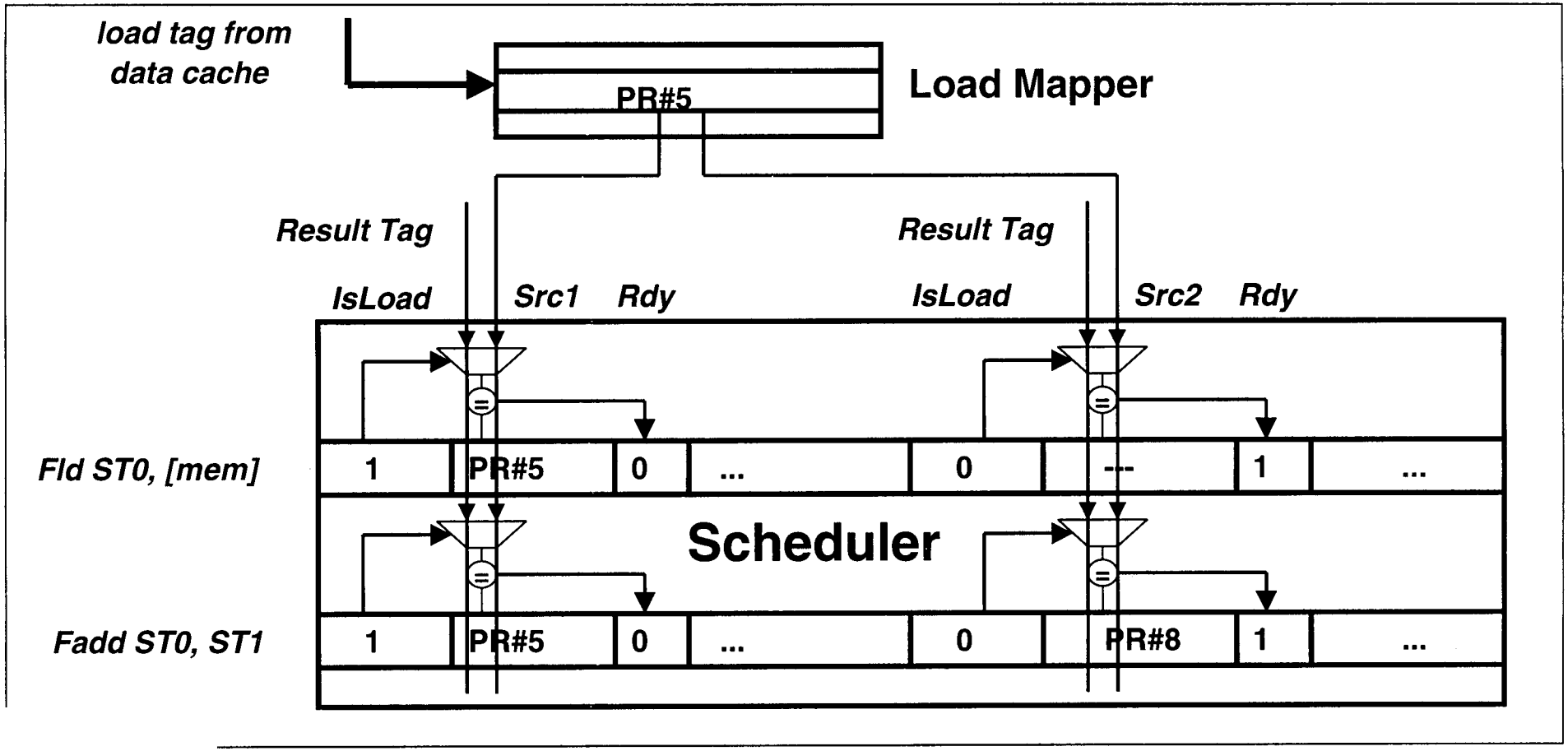


Scheduler

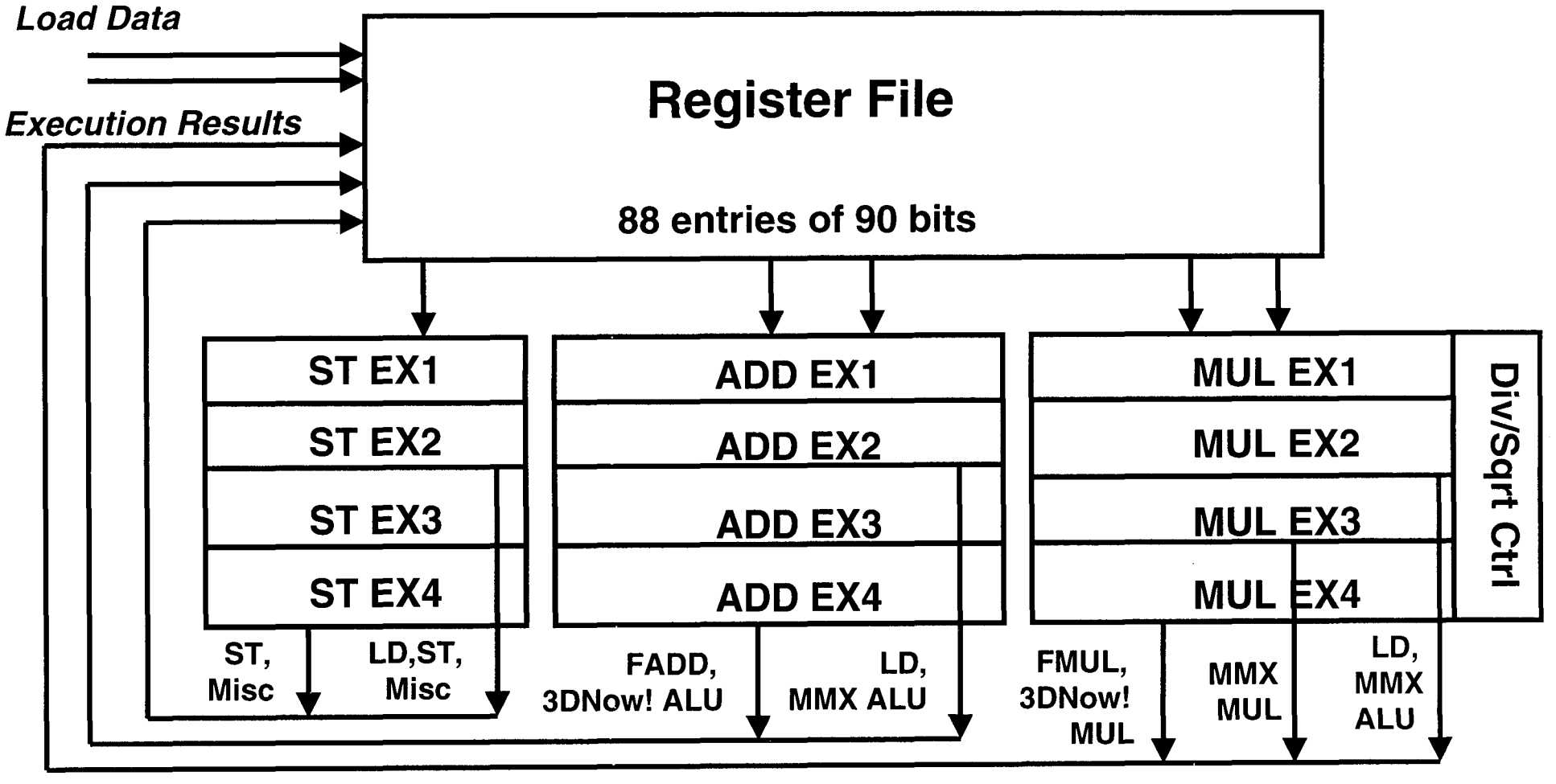
- Depth is 12 by 3 entries
- Op has exec type and latency when written
- Oldest "ready" op issued to each of 3 exec pipes each cycle
- Entries become available for new ops once issued
- Load data "super" bypassed to dependent ops

"Super" Bypass of Load Data

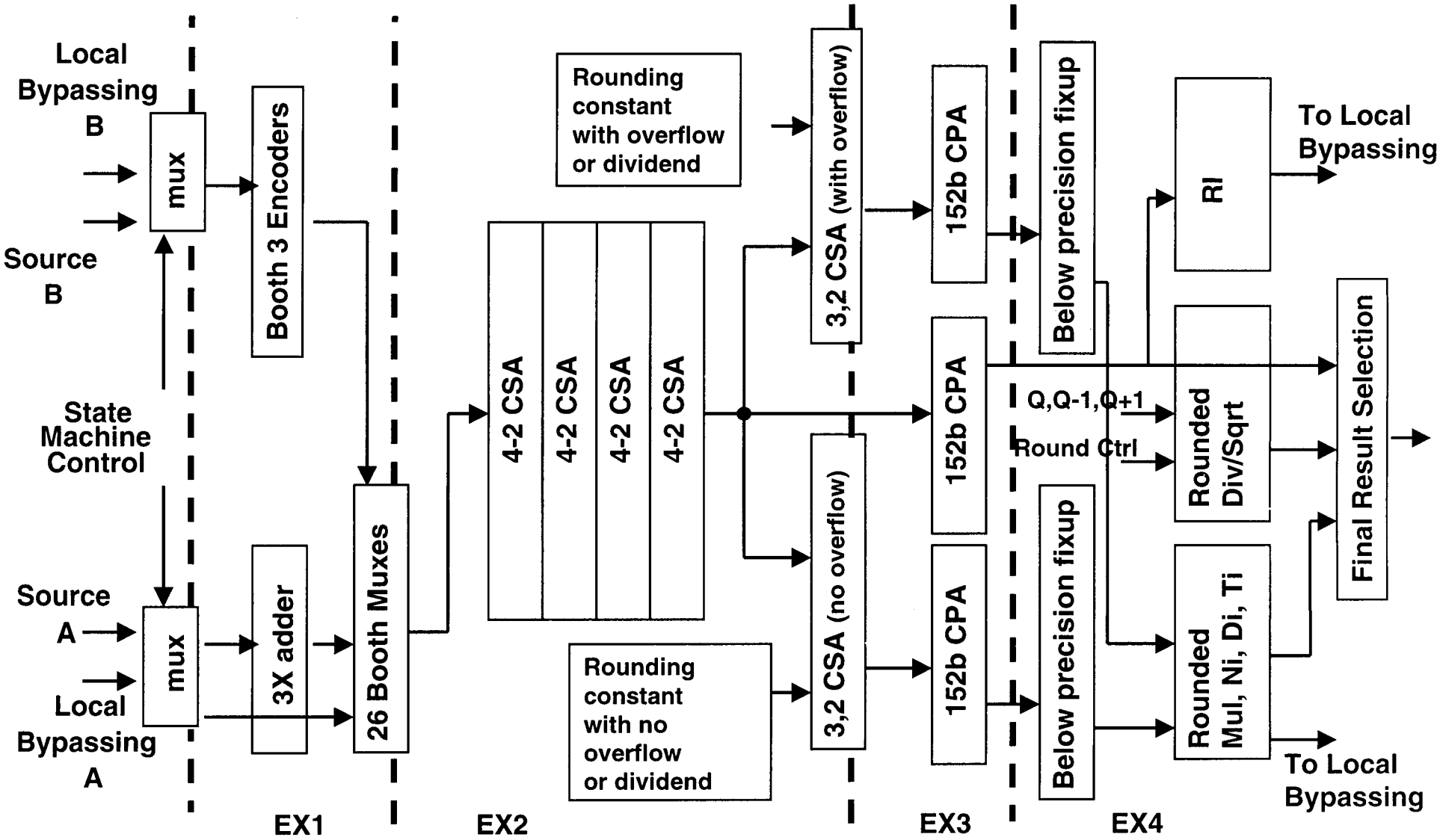
- (1) FLD ST0, [mem] : FLD [mem] -> PR#5
- (2) FADD ST0, ST1 : FADD PR#5, PR#8 --> PR#12
- Goal is to forward load data directly to instruction (2)



Execution Units

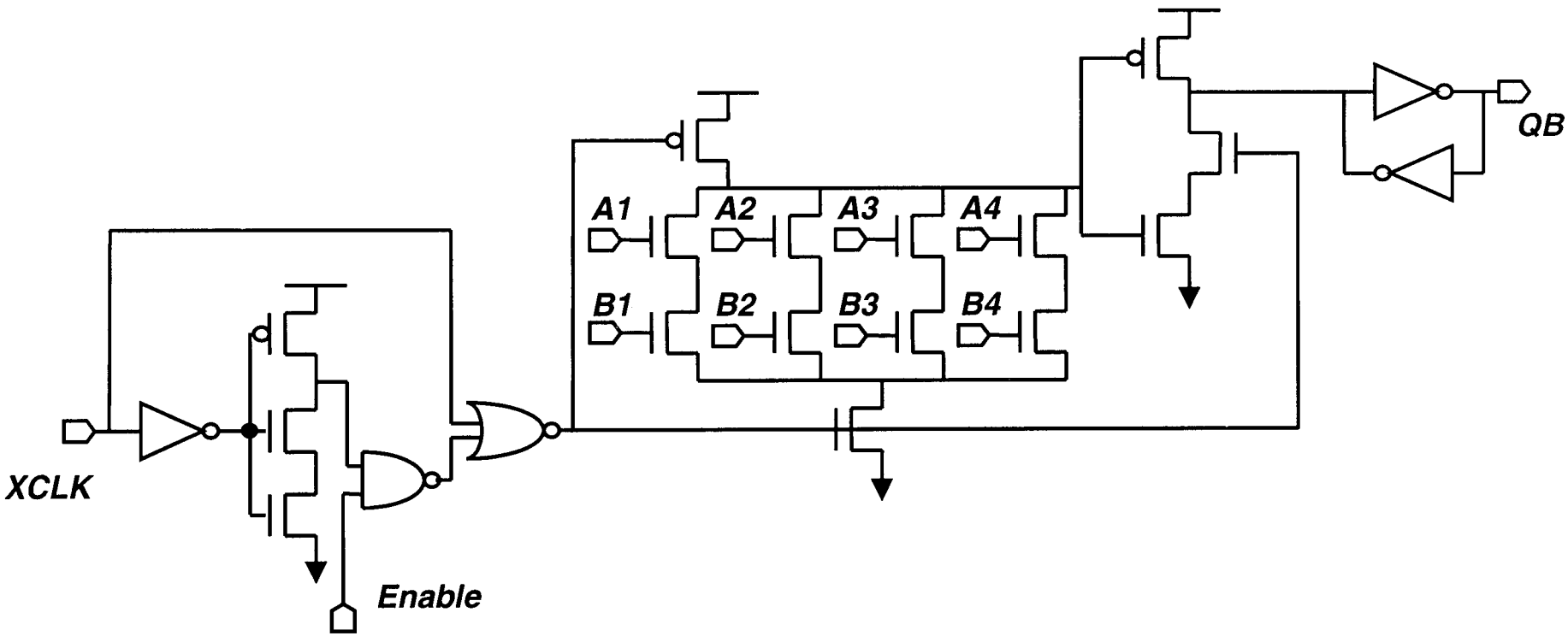


Multiplier Organization



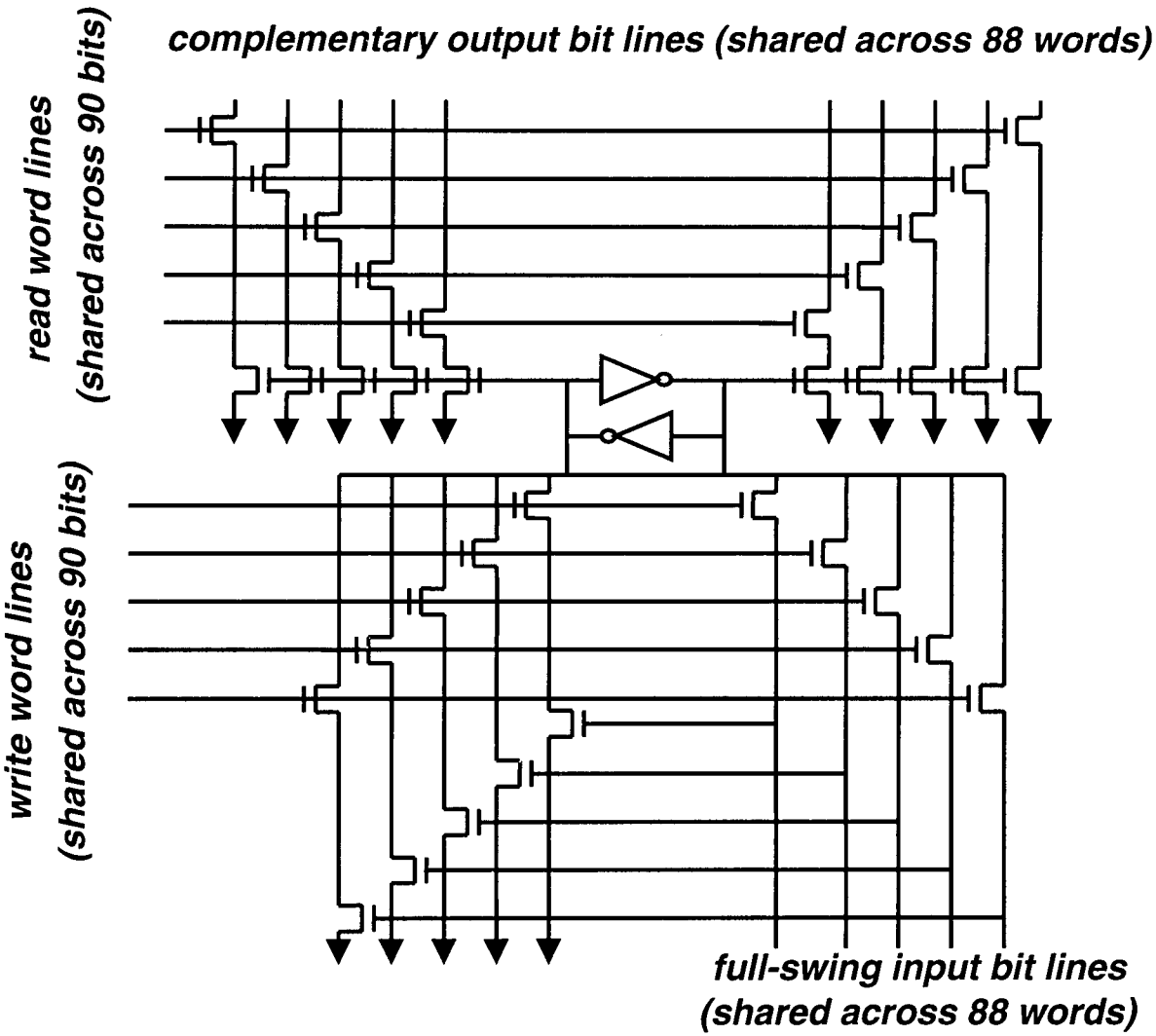
Logic Flops

- Flop design allowed complex logic on input stage with minimal performance penalty
- Used extensively in datapaths to reduce area and increase frequency

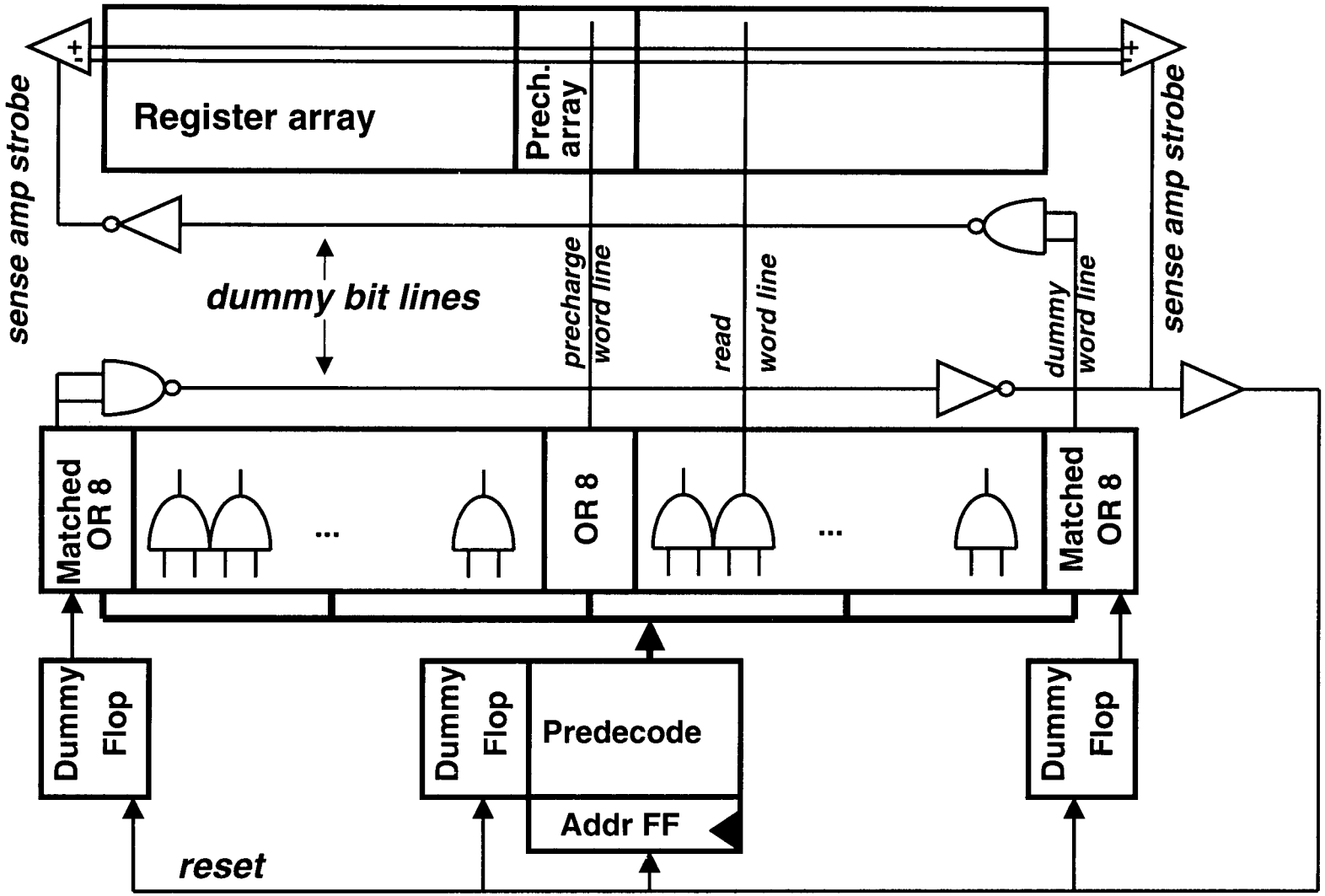


Example logic flop -- 4:1 mux with enable

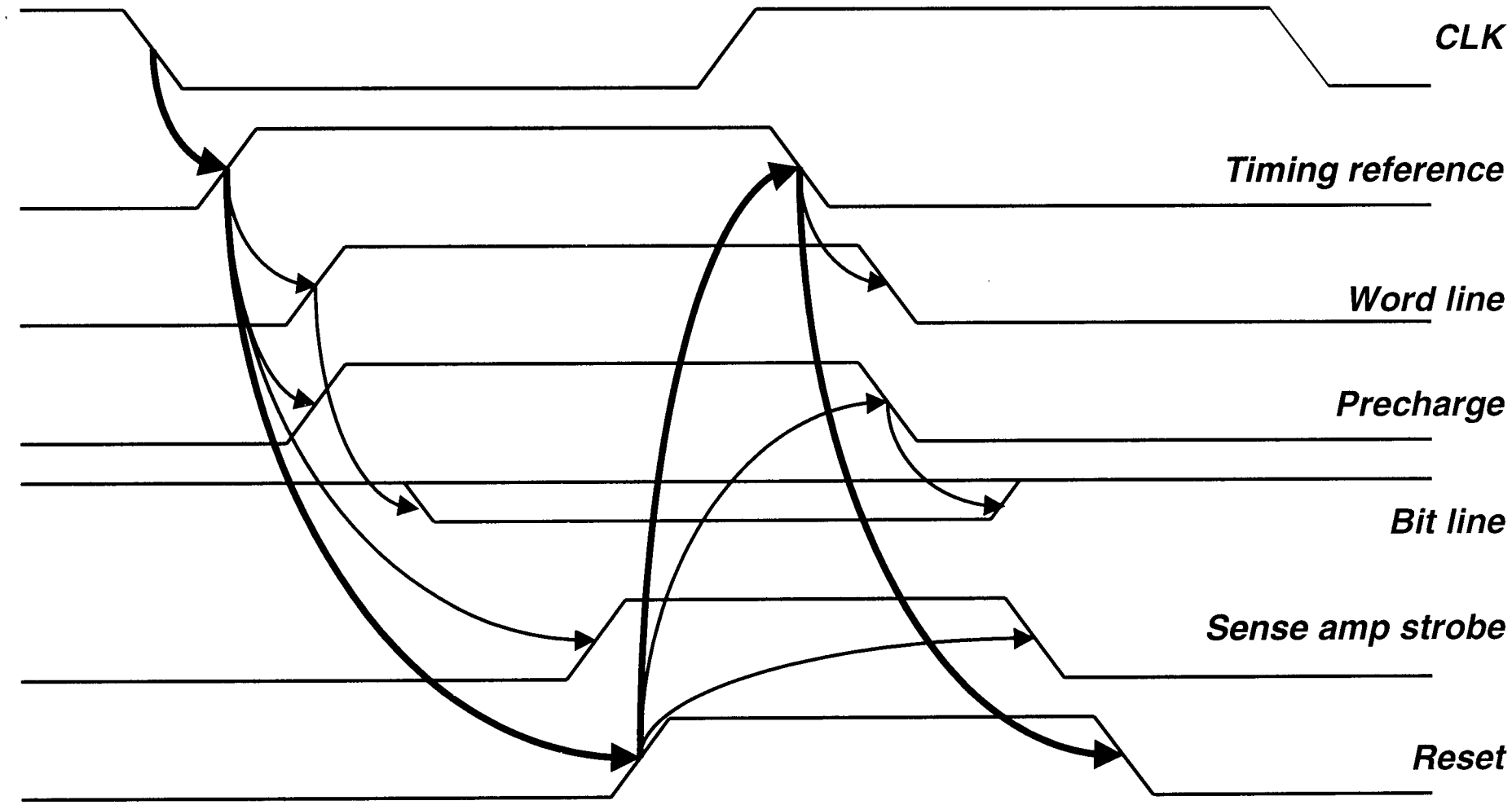
Register File Bit Cell



Register File Block Diagram



Register File Timing Signals



Cell Based Design Methodology

- Unit composed of more than 150K standard cells making up 80% by area
- Design partitioned and floorplan made top-down
- Blocks designed bottom-up
- Automatic tools used to best effect in place and route
- Route parasitics extracted and used in static timing

Cell Library

- Cell library developed by design team
- Library cells characterized by custom tools to reflect the chip usage environment
- Rules established for cells requiring restricted usage
- Rules checked statically at the appropriate point in the design flow
  - ie. driver size rules checked after gate netlist is generated and coupling rules checked after extraction is complete

Timing Methodology

- Global timing database with negotiated constraints established early in design process
- Allows top-down design partitioning and bottom-up design and assembly of blocks
- Static timing analysis includes parasitics and coupling effects
- Hold time checked with conservative expectations and process margin on race paths

Summary

- Presented an integrated floating-point multimedia unit for an x86 microprocessor
- Careful use of cell-based design with custom macros allowed for timely completion of project
- The out-of-order superscalar architecture and selectively aggressive circuit design enables a processor for high-end x86 computer systems